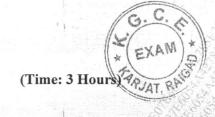
## Paper / Subject Code: 51402 / Logic Design

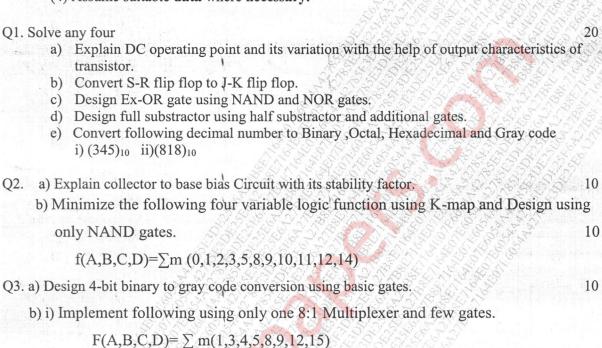
S.E. SEM III / IT / CHOICE BASED / MAY 2019 / 14.05.2019



[Total Marks: 80]

 N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions out of remaining five.
(2) Fig. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.

- (3) Figures to **right** indicate **full** marks.
- (4) Assume suitable data where necessary.



ii) With neat logic diagram explain in short operation of Universal Shift Register.	10
Q4. a) Design a Mod 10 synchronous counter using J-K Flipflop.	10
b) Using Quine MC Cluskey Method determine Minimal SOP form for	10
$F(A,B,C,D) = \sum m(0,1,2,5,6,7,8,9,10,14)$	

Q5. a) Explain about ENTITY declarations in VHDL and write VHDL program for NAND a	ind
OR gates.	10
b) Implement 3 bit asynchronous up counter and also sketch the timing diagram.	10
Q6 Solve the following-	20

- a) Explain working of 8:1 Multiplexer.
- b) Working of S-R flip flop(with its internal circuit diagram and truth table).
- c) Explain working of Constant Current source.
- d) Write VHDL program for full substractor.